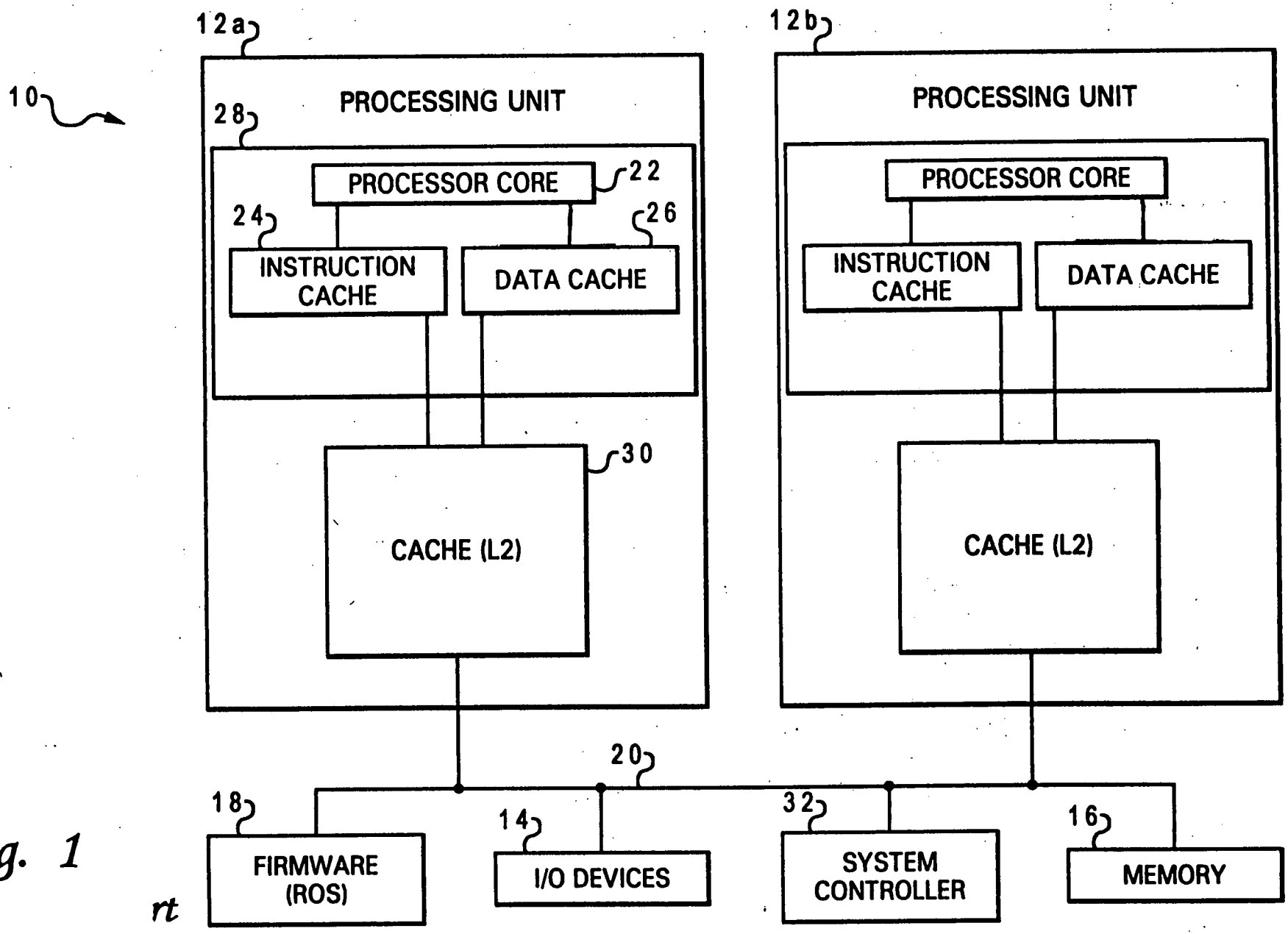


Fig. 1

rt

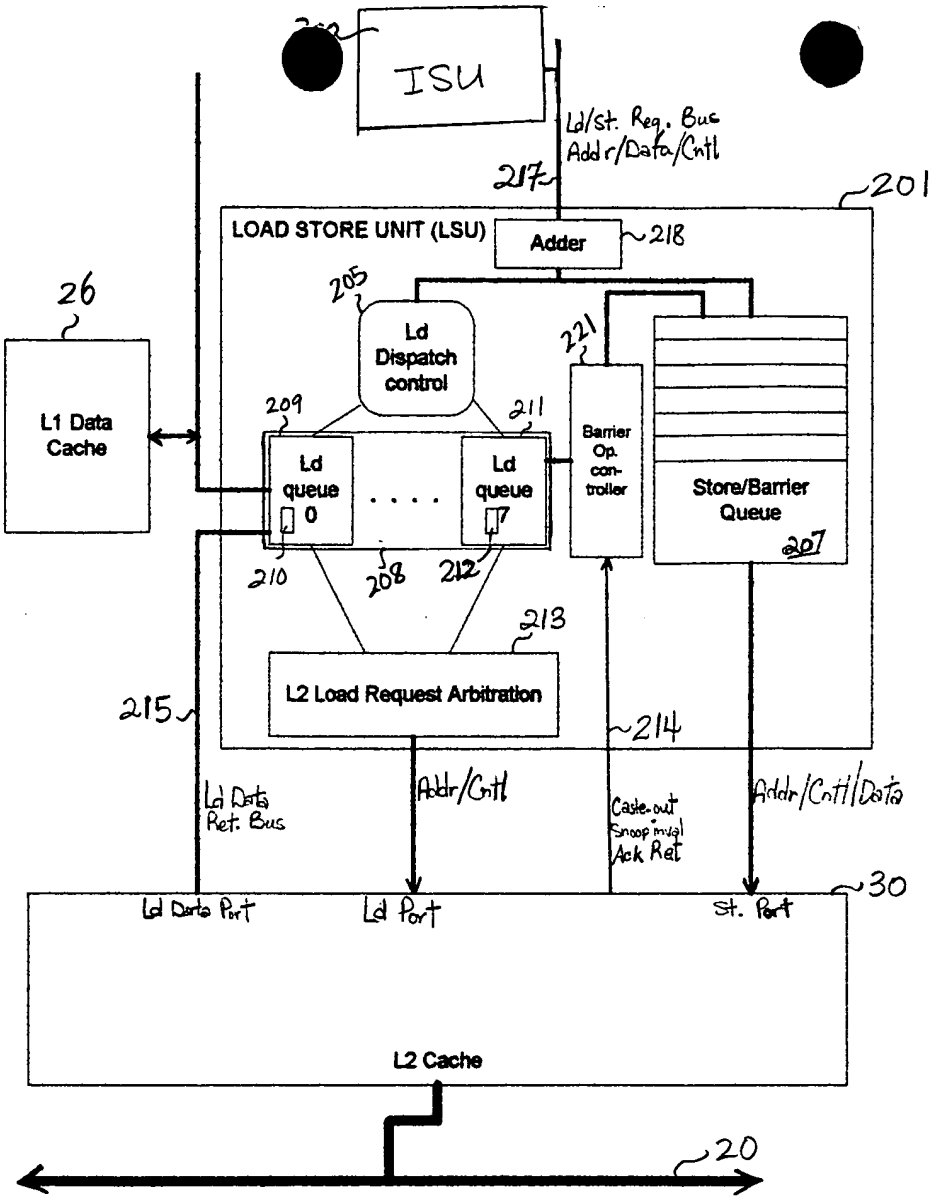

ISU
Ld/St. Req. Bus
Addr/Data/Cntl
217
201
LOAD STORE UNIT (LSU)
Adder
218
205
Ld
Dispatch
control
221
26
L1 Data
Cache
209
211
Ld
queue
0
Ld
queue
Barrier
Op.
con-
troller
Store/Barrier
Queue
207
210
208
212
213
L2 Load Request Arbitration
215
214
Ld Data
Ret. Bus
Addr/Cntl
Castout
Snoop inval
Ack Ret
Addr/Cntl/Data
30
Ld Data Port
Ld Port
St. Port
L2 Cache
20

FIG. 2

FIG. 3A

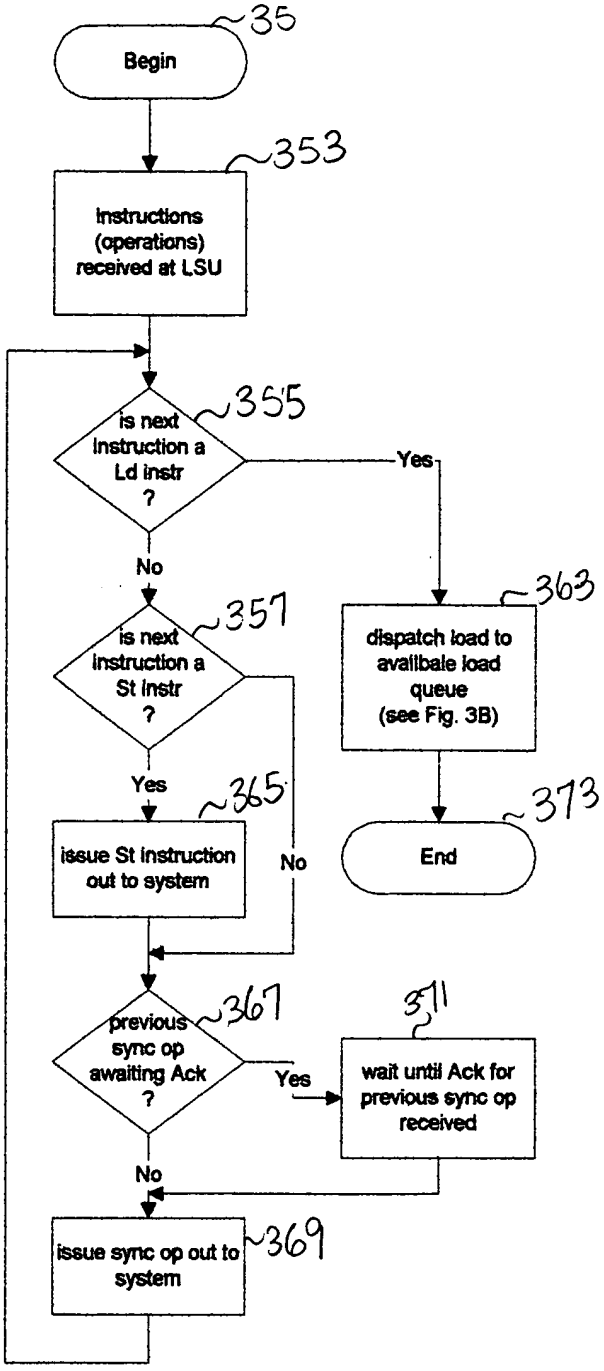

Begin
35
Instructions (operations) received at LSU
353
is next instruction a Ld instr ?
355
Yes
No
is next instruction a St instr ?
357
Yes
No
issue St instruction out to system
365
dispatch load to availbale load queue (see Fig. 3B)
363
End
373
previous sync op awaiting Ack ?
367
Yes
No
wait until Ack for previous sync op received
371
issue sync op out to system
369

FIG. 3B

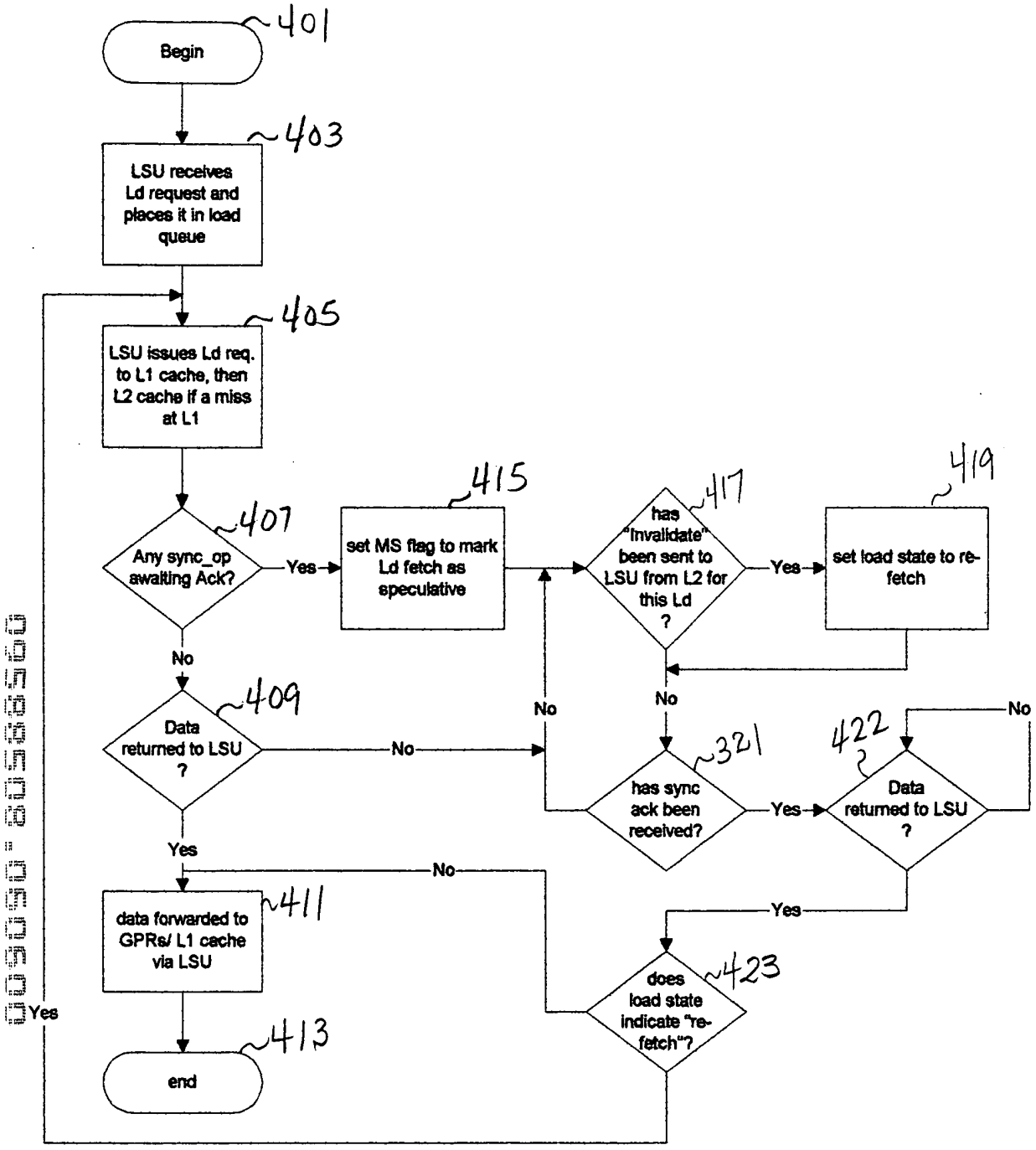

Begin
401
LSU receives Ld request and places it in load queue
403
LSU issues Ld req. to L1 cache, then L2 cache if a miss at L1
405
Any sync_op awaiting Ack?
407
Yes
set MS flag to mark Ld fetch as speculative
415
has "invalidate" been sent to LSU from L2 for this Ld ?
417
Yes
set load state to re-fetch
419
No
Data returned to LSU ?
409
No
No
has sync ack been received?
321
Yes
Data returned to LSU ?
422
No
Yes
No
data forwarded to GPRs/ L1 cache via LSU
411
Yes
does load state indicate "re-fetch"?
423
Yes
end
413

FIG 4A

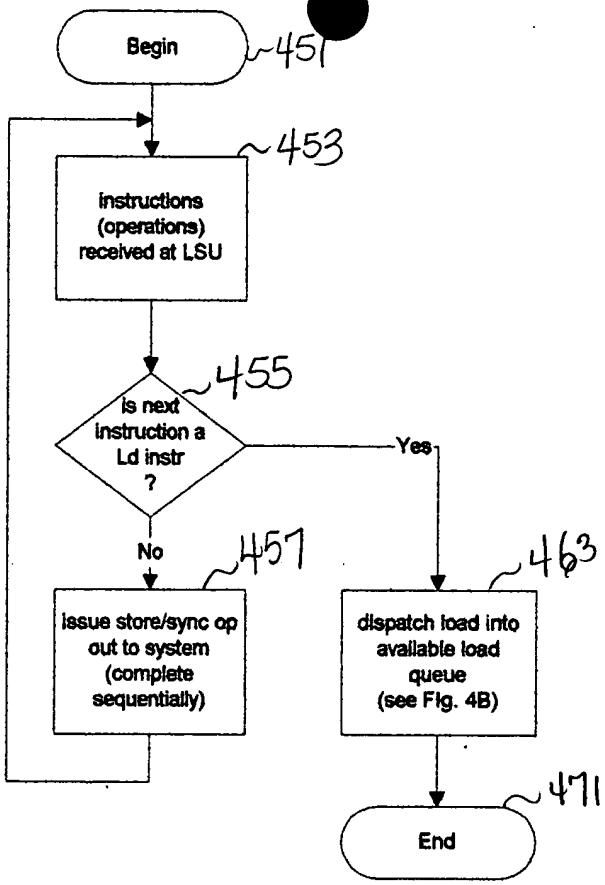


FIG. 4B

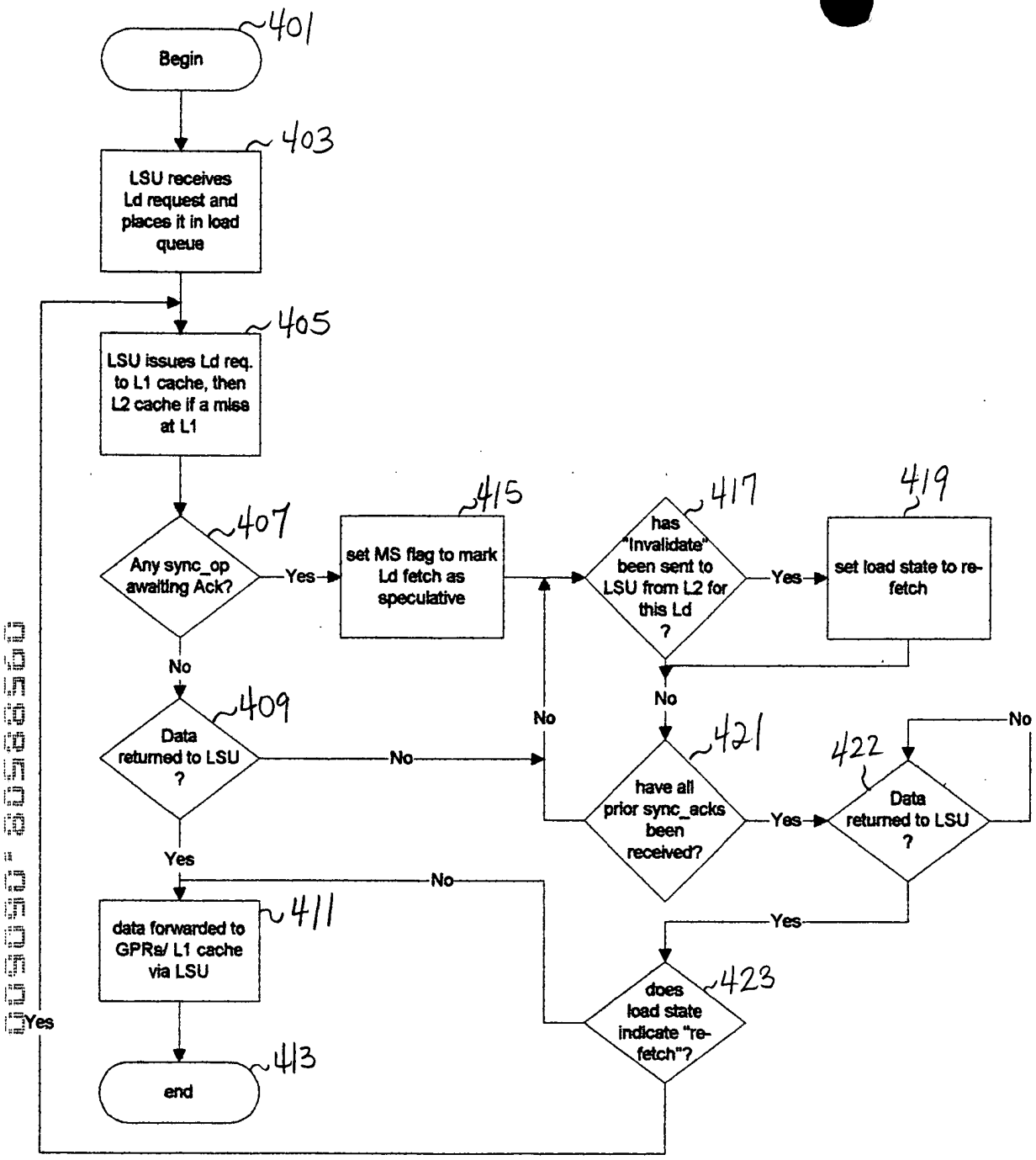

401
Begin
403
LSU receives Ld request and places it in load queue
405
LSU issues Ld req. to L1 cache, then L2 cache if a miss at L1
407
Any sync_op awaiting Ack?
Yes
No
415
set MS flag to mark Ld fetch as speculative
417
has "Invalidate" been sent to LSU from L2 for this Ld ?
Yes
No
419
set load state to re-fetch
409
Data returned to LSU ?
No
Yes
421
have all prior sync_acks been received?
Yes
No
422
Data returned to LSU ?
No
Yes
411
data forwarded to GPRs/ L1 cache via LSU
423
does load state indicate "re-fetch"?
Yes
No
413
end
Yes

FIG. 5

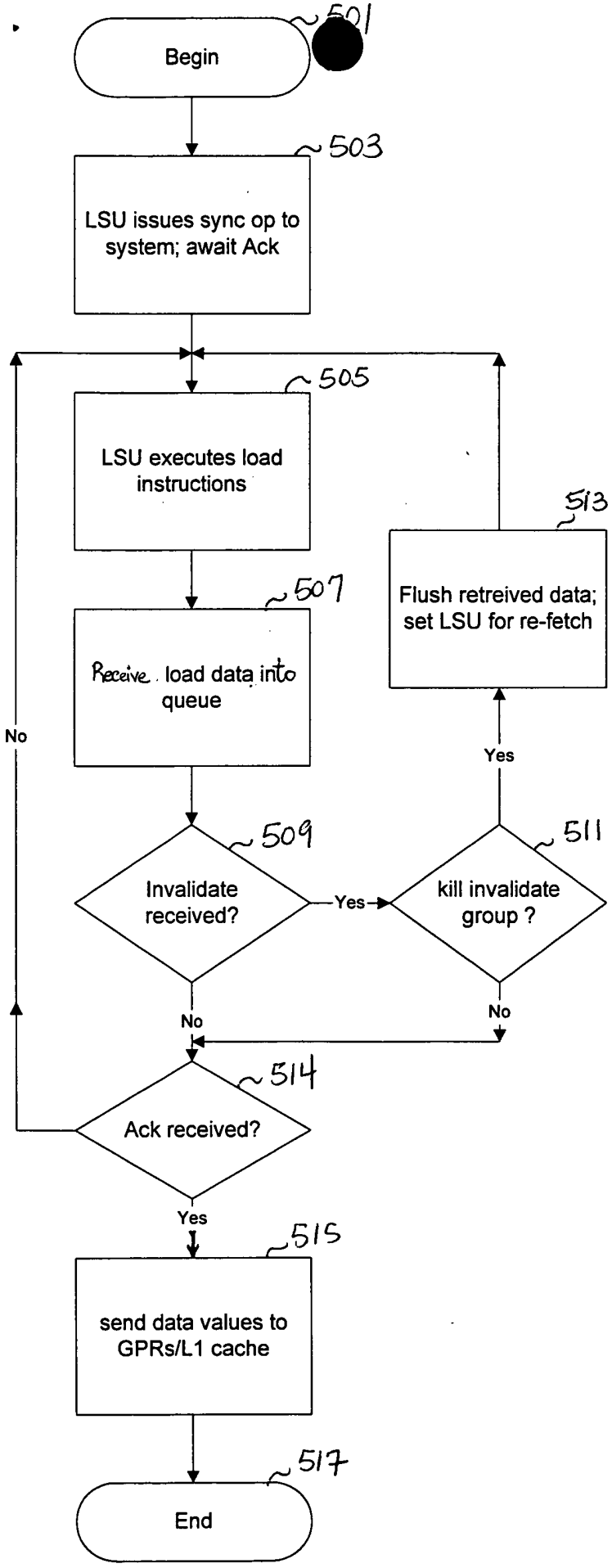

501
Begin
503
LSU issues sync op to system; await Ack
505
LSU executes load instructions
507
Receive load data into queue
509
Invalidate received?
Yes
511
kill invalidate group ?
513
Flush retreived data; set LSU for re-fetch
Yes
No
No
No
514
Ack received?
Yes
515
send data values to GPRs/L1 cache
517
End

FIG. 8

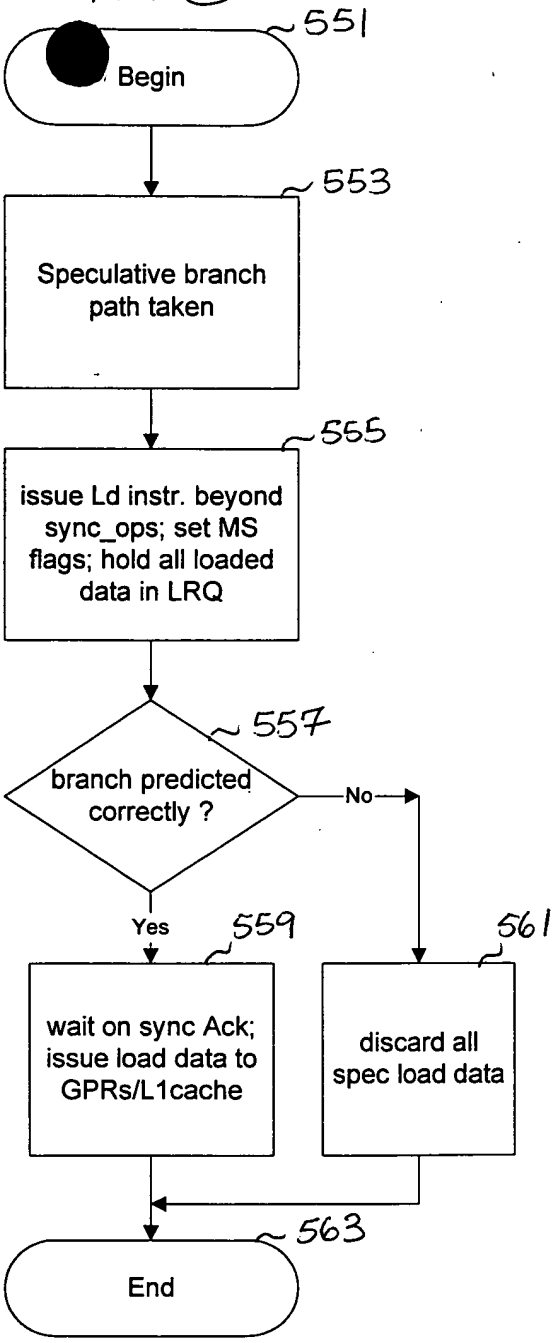

551
Begin
553
Speculative branch path taken
555
issue Ld instr. beyond sync_ops; set MS flags; hold all loaded data in LRQ
557
branch predicted correctly ?
No
Yes
559
wait on sync Ack; issue load data to GPRs/L1cache
561
discard all spec load data
563
End

FIG. 6A

1) St-An [GROUP A]
2) Ld-A0
3) Ld-An
4) Sync A
5) Ld-B0 [GROUP B]
6) Ld-Bn
7) St-Bn

FIG. 6B

1) Ld-A0
2) Ld-A1
3) St-An
4) Sync-A
5) Ld-B0
6) Ld-B1
7) St-Bn
8) Sync-B
9) Ld-C0
10) Ld-C1
11) St-Cn
12) Sync-C
13) Ld-C0
14) Ld-C1
15) St-Bn
16) Sync-D

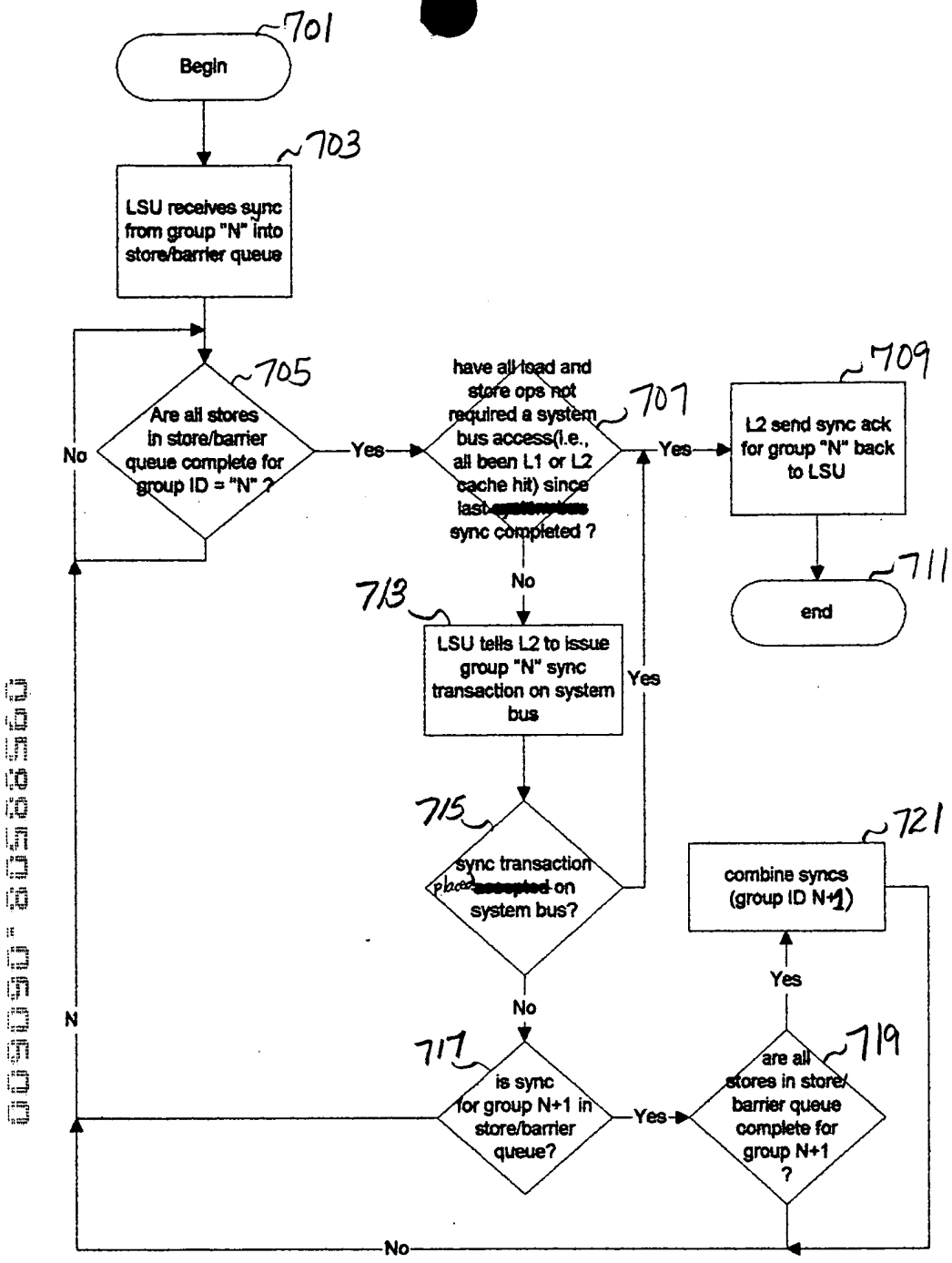
FIG. 6C

Proc Issue Order	LSU Order to Memory Subsystem	Memory Subsystem Execution order	LSU Completion Order
1) Ld-A0	1) Ld-A0 Sync-A	1) Ld-B0	1) Ld-A0
2) Ld-b0	2) Ld-b0 Sync-B	2) Ld-d0	2) Ld-B0
3) St-C0	3) St-C0 Sync-C	3) Ld-A0	3) St-C0
4) Ld-D0	4) Ld-D0 Sync-D	4) St-C0 5) Sync A,B,C,D	4) Ld-D0

FIG. 6D

Instruction Order	Memory Subsystem Execution Order
St-A0	St-A0
St-A1	St-A1
Sync-A	St-B0
St-B0	St-B1
St-B1	Sync A and B
Sync-B	

FIG. 7


701
Begin
703
LSU receives sync from group "N" into store/barrier queue
705
Are all stores in store/barrier queue complete for group ID = "N" ?
No
Yes
have all load and store ops not required a system bus access(i.e., all been L1 or L2 cache hit) since last sync completed ?
707
Yes
No
709
L2 send sync ack for group "N" back to LSU
711
end
713
LSU tells L2 to issue group "N" sync transaction on system bus
Yes
715
sync transaction placed on system bus?
No
717
is sync for group N+1 in store/barrier queue?
Yes
719
are all stores in store/barrier queue complete for group N+1 ?
Yes
721
combine syncs (group ID N+1)
No
No